REMARKS

Claims 1-20 were examined. Claims 1-5, 7 and 19-20 are allowed. Claims 6, 10, 14 and 15 are rejected. Claims 8-9, 11-13 and 16-18 are objected to as allowable if rewritten in independent form. Applicants amend no claims. Applicants respectfully request reconsideration of claims 6, 10, 14 and 15, in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. § 102

The Patent Office rejects claims 6, 10, 14 and 15 under 35 U.S.C § 102(b) as being anticipated by U.S. Patent No. Re. 35,064 issued to Hernandez (Hernandez) (U.S. Patent No. 5,095,626 to Kitamura et al. (Kitamura) is used by the Examiner as evidence that dual in-line IC package of the type disclosed in Hernandez comprises an IC mounted on an IC package that carries the IC and leads). It is axiomatic that to be anticipated every limitation of a claim must be disclosed in a single reference.

Applicants respectfully disagree with the rejection above and submit that independent claims 6 and 15 are patentable over the cited reference for at least the reason that the reference does not disclose an array capacitor underneath an integrated circuit and having openings to enable pins from an integrated circuit package to pass through as required by claims 6 and 15.

The Patent Office relies upon Hernandez to disclose openings to enable pins from an integrated circuit (IC) package to pass through, as required by claims 6 and 15. Hernandez describes leads 112 which are mounted in plated through holes 114 in multilayer circuit board 90A. Where plated through holes 114 are provided to interconnect circuit patterns 98 and 100 only two outer surfaces of the board (*see*, col. 6, lines 48-58). On the other hand, as described in Applicants' specification, according to embodiments, without limitation thereto, "openings" such as openings 155 of Figure 2 may enable pins (such as pins 135 of Figure 2) to pass through capacitor 140 without contacting conductive layers 201, 202, etc. due to distance or space 160 between the pins and the conductive layers, as shown in Figure 2. Specifically, in some embodiments, without limitation thereto, the claimed arrangement allows the pins to pass through the capacitor through a low resistance path through the capacitor such as described in paragraph [0016] and shown in Figure 2 of the application. However, Hernandez does

not disclose "openings to enable pins...to pass through," as claimed, but instead describes leads "mounted in plated through holes" so that the plated through holes provide interconnection between the leads and interconnection circuit patterns 98 and 100 to provide contacts to the interconnect circuit patterns for circuit board 90A of Figure 11 similar to those for circuit board 90 of Figures 9 and 10 (*see*, col. 6, lines 53-58).

Similarly, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Kitamura of the above-noted "openings to enable pins from an integrated circuit package to pass through" limitations of claims 6 and 15.

Consequently, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Hernandez or Kitamura of an array capacitor underneath an integrated circuit and having openings to enable pins from the integrated circuit package to pass through, as required by claims 6 and 15. Hence, for at least this reason, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

In addition to the reasons above, Applicants disagree with the rejection above for dependent claim 10 for at least the reason that the cited references do not disclose openings having a diameter which is greater than a diameter of the pins, such that a defined distance is maintained between an edge of each opening and each pin, as required by claim 10.

An argument analogous to the one above applies here as well. Specifically, Hernandez describes the pins mounted in the through holes. Similarly, Kitamura does not disclose the above noted limitation of claim 10. Consequently, the Patent Office has not identified and Applicants are unable to find any disclosure in the cited references of the above-noted limitation of claim 10. Hence, for at least this additional reason, Applicants respectfully request the Patent Office withdraw the rejection above of claim 10.

II. Allowable Subject Matter

Applicants note with appreciation that the Patent Office has indicated that claims 1-5, 7, and 19-20 are allowed over the prior art of record, and that claims 8-9, 13-15 and 16-18 are objected to as allowable if rewritten in independent form.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office.

Suzanne Johnston 2/7/07
Date